SRI VENKATESWARA COLLEGE OF ENGINEERING

(AUTONOMOUS)

Karakambadi Road, Tirupati-517507

R20

EXAMINATION BRANCH

M.Tech II Semester (R20) Supplementary Examinations October-2025

TIME TABLE

Exam Timings: **9.30 AM TO 12.30 PM**

Date/Day	VLSI Design (VLSI D)	Computer Science and Engineering (CSE)
06-10-2025 (Monday)	CMOS Mixed Signal Design (EC20DPC201)	Advanced Algorithms (CS20DPC201)
08-10-2025 (Wednesday)	Physical Design Automation (EC20DPC202)	Advanced Computer Architecture (CS20DPC202)
10-10-2025 (Friday)	MEMS System Design (EC20DPE205)	Network Security (CS20DPE203)
14-10-2025 (Tuesday)	Low power VLSI Design (EC20DPE206)	Human Computer Interaction (CS20DPE206)

Note: Any discrepancy in this time table may be brought to the notice of the under signed immediately.

Controller of Examinations **Dy Chief Superintendent** **Principal**

Date: 22-09-2025